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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/491,302	01/25/2000	John D. Geissinger	55271USA6A	8370

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EXAMINER
BROCK II, PAUL E

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/01/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/491,302	GEISSINGER ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

P riod for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *5-7 and 20-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 8-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 January 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Election/Restrictions

1. Claims 5 – 7 and 20 – 26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group and species, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 9.

Oath/Declaration

2. The Affidavit filed on September 19, 2002 under 37 CFR 1.131 has been considered but is ineffective to overcome the Fujisawa reference.

3. The evidence submitted is insufficient to establish a conception of the invention prior to the effective date of the Fujisawa reference. While conception is the mental part of the inventive act, it must be capable of proof, such as by demonstrative evidence or by a complete disclosure to another. Conception is more than a vague idea of how to solve a problem. The requisite means themselves and their interaction must also be comprehended. See *Mergenthaler v. Scudder*, 1897 C.D. 724, 81 O.G. 1417 (D.C. Cir. 1897). The evidence does not show the whole invention as claimed for at least the reason that an interconnect member connected between each of the conductive layers of the capacitor is not shown.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1 – 4, and 8 – 19 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. It is not clear where in the originally filed specification support for "an internal capacitor" can be found. While the applicant has pointed out that support for "an internal capacitor" "appears in the specification at, e.g., p.1., lines 1-2 (integrated capacitor) and Fig. 3, 5, and 6," it is not clear that a recitation of an "integrated capacitor" provides support for "an internal capacitor." Nor is it clear how figures 3, 5, and 6, which depict an integrated capacitor, depict support for "an internal capacitor."

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

It is not clear if the limitation "the non-conductive polymer is blended with high dielectric constant particles" is referring to the same "high dielectric constant particles as

claimed in claim 1. For purposes of this office action "the non-conductive polymer is blended with high dielectric constant particles" will be considered -- the high dielectric constant particles are --.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1 – 3, 8 – 13 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto et al. (USPAT 5883428, Kabumoto) in view of Brandt et al. (USPAT 6068782, Brandt) and Parker et al. (USPAT 5633785, Parker).

Kabumoto discloses in figure 1 an electronic package (4). Kabumoto discloses in figure 1 a conductive trace layer (5) having a first side and a second side, the conductive trace layer being patterned to define a plurality of interconnect pads (5a and 5b). Kabumoto discloses in figure 1 a dielectric substrate (portion of 1 above 5) mounted on the first side of the conductive trace layer. Kabumoto discloses in figure 1 an internal capacitor including a first conductive layer (10), a second conductive layer (11) and a layer of dielectric material (portion of 1 between 10 and 11) disposed between the first and the second conductive layers, the first conductive layer attached to the second side of the conductive trace layer by a first adhesive layer (portion of 1

between 10 and 5). Kabumoto does not disclose that the dielectric material is made of a non-conductive polymer blended with high dielectric particles. Brandt discloses in column 4, lines 18 – 41 a dielectric material made of a non-conductive polymer blended with high dielectric particles. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric material of Brandt in the method of Kabumoto in order to tune the electronic properties of a capacitor component as stated by Brandt in column 4, lines 22 – 41. Kabumoto and Brandt are silent to the capacitor having a capacitance of from about 1 nf/sq.cm. to about 100 nf/sq.cm. Parker teaches in figure 4, column 5, lines 43 – 50 and column 7, lines 4 – 12 a capacitor with a capacitance of about 10 nf/sq.cm. It would have been obvious to one of ordinary skill in the art at the time of the present invention to have the capacitance of Parker in the package of Kabumoto and Brandt in order to provide a capacitance which is sufficient for capacitive decoupling in a package as stated by Parker in column 7, lines 8 – 12. Kabumoto discloses in figure 1 a plurality of interconnect regions (12a – 12d) extending through the first conductive layer and the dielectric material layer of the capacitor. Kabumoto discloses in figure 1 an interconnect member connected between each of the conductive layers of the capacitor and a corresponding set of the interconnect pads, the first conductive layer of the capacitor being electrically connected (12a) to a first set of the interconnect pads and the second conductive layer on the capacitor being electrically connected (12b) to a second set of the interconnect pads, the interconnect members corresponding to the second set of interconnect pads extending through one of the interconnect regions.

With regard to claim 2, Kabumoto discloses in column 5, lines 23 – 34 wherein the first electrode is maintained at a first reference voltage and wherein the second electrode is maintained at a second reference voltage different from the first reference voltage.

With regard to claim 3, Kabumoto discloses in figure 1 an electrically conductive stiffening member (H) attached to the second conductive layer of the capacitor by a second adhesive layer (portion of 1 between H and 11).

With regard to claims 8 – 10, Parker discloses in column 7, lines 8 – 12 a capacitor that has a capacitance of from about 5 nF/sq.cm. to about 30 nF/sq.cm. or of at least 30 nF/sq.cm.

With regard to claim 11, Brandt teaches in column 4, lines 35 – 37 wherein the dielectric material of a capacitor has a thickness of 10 um. It would have been further obvious to one of ordinary skill in the art at the time of the present invention to use the dielectric thickness of Brandt in the device of the present combination in order to have a useful thickness for a dielectric layer of a capacitor in a semiconductor package as stated by Brandt in column 4, lines 35 – 37.

With regard to claim 12, Brandt discloses in column 4, lines 18 – 41 wherein the dielectric material of the capacitor includes a metal oxide.

With regard to claim 13, Brandt discloses in column 4, lines 18 – 41 the high dielectric constant particles are formed from a material of lead zirconium titanate.

With regard to claim 17, Kabumoto discloses in figure 1 wherein the interconnect member is a solder plug.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto, Brandt, and Parker as applied to claims 1 and 3 above, and further in view of Dehaine et al. (USPAT 4982311, Dehaine).

Kabumoto discloses in figure 1 a device receiving region extending through the dielectric substrate and the conductive trace layer and further comprises an electronic device (3) attached to the device receiving region on the stiffening member by a third adhesive layer (1a). Kabumoto, Brandt and Parker are silent to the device-receiving region also extends through the capacitor and further comprises the electronic device mounted on the stiffening member. Dehaine discloses in figure 1 a device receiving region extending through a dielectric substrate (16), a conductive trace layer (34b), a capacitor (18a and 18b), and further comprises an electronic device (12) attached to the device receiving region on a stiffening member (20) by a third adhesive layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the receiving region of Dehaine in the device of Kabumoto, Brandt, and Parker in order to allow easy refrigeration of the electronic device as stated by Dehaine in column 2, lines 33 – 40. It is known that electronic devices such as semiconductor elements run more efficiently at reduced temperatures.

11. Claims 14 – 16, 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto, Brandt, and Parker as applied to claim 1 above, and further in view of Fujisawa et al. (USPAT 6184567, Fujisawa).

With regard to claim 14, Kabumoto discloses in figure 1 wherein the dielectric substrate includes a plurality of apertures, at least one of the apertures being positioned adjacent to one of

the interconnect region of the capacitor. Kabumoto, Brandt, and Parker do not disclose that the dielectric substrate includes a plurality of apertures, each one of the apertures being positioned adjacent to one of the interconnect region of the capacitor. Fujisawa teaches in figure 8 wherein a dielectric substrate (12) includes a plurality of apertures, each one of the apertures being positioned adjacent to one of an interconnect regions of a capacitor. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the plurality of apertures of Fujisawa in the device of Kabumoto, Brandt, and Parker in order to ensure insulation between contact pads of the trace layer.

With regard to claims 15 and 16, Kabumoto discloses in figure 1 and column 4, lines 7 – 19 wherein the dielectric substrate includes aluminum oxide. Kabumoto, Brandt, and Parker do not disclose that the dielectric substrate includes a polymeric film that is a polyimide film. Fujisawa teaches in column 3, line 19 wherein a dielectric substrate includes a polymeric film that is a polyimide film. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the polyimide film of Fujisawa in the device of Kabumoto, Brandt, and Parker in order to resist metallization while bonding to the electronic device.

With regard to claim 18, Kabumoto discloses in figure 1 wherein each interconnect pad is a wire pad. Kabumoto, Brandt, and Parker do not disclose wherein each interconnect pad is a solder pad. Fujisawa teaches in figure 8 interconnect pad (28 and 32) is a solder pad. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the solder pad of Fujisawa as the interconnect pad in the device of Kabumoto, Brandt, and Parker in order to use flip chip bonding for the connection.

With regard to claim 19, Kabumoto discloses in figure 1 wherein the dielectric substrate has an aperture extending therethrough adjacent each interconnect pad. It would have been further obvious in the method of Kabumoto, Parker and Fujisawa that the dielectric substrate has an aperture extending therethrough adjacent each solderball pad.

Response to Arguments

12. Applicant's arguments filed March 4, 2003 have been fully considered but they are not persuasive.

13. With regard to the applicant's argument that "Kabumoto teaches away from using internal capacitors to achieve higher capacitance," it should be noted that the capacitor in figure 1 of Kabumoto is an internal capacitor. Further, the phrase "to achieve higher capacitance" appears to be a relative phrase that does not relate the claimed capacitor to the capacitor of Kabumoto. It is not clear what the capacitance is higher than. Therefore the applicant's argument is not persuasive, and the rejection is proper.

14. With regard to the applicant's arguments that "there is no motivation to use the high capacitance internal capacitor of Parker in the Kabumoto structure," it should be noted that the internal capacitor of Parker is not being substituted into the Kabumoto structure. In fact, Parker is being used in combination with Kabumoto and Brandt to show that an internal capacitor can have a capacitance of the claimed range. For example, Kabumoto and Brandt are silent to the

capacitance of their capacitor. Therefore the applicant's argument is not persuasive, and the rejection is proper.

15. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
March 27, 2003

EDDIE LEE
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